Integrated 150 GHz Silicon IMPATT Diodes for Power Combining Applications

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Abstract - This paper describes the manufacturing process of integrated Si-IMPATT diodes for power combining applications at 150 GHz.
A computer optimized doping profile is grown by molecular beam epitaxy (MBE) on high resistivity Si-substrate. The new technology process that realizes the integration of a diode and its housing is explained in detail. The device is thermo-compression bonded in a single step onto a diamond heat sink. Measurements are made in a rectangular, reduced height waveguide resonator.
The integrated IMPATT device is designed for high reproducibility. Variations that were formerly introduced by multiple bonding steps in the fabrication of quartz ring housings are eliminated. The single bonding step used here results in the improved diode matching required for power combining applications.

I. INTRODUCTION

Limited DC-power dissipation and a suitable packaging technology are barriers to building high power IMPATT diodes. Especially at millimeter-wave frequencies, optimization of both doping profile and mounting of the diode is important.
The most efficient doping profile is a double Read (DLHL) structure which reduces the operating voltage. This allows a higher current density through the diode compared to a flat double drift (DD) design. The doping profile is computer optimized for a low breakdown voltage and high negative resistance using an existing simulation tool that is based on a hydro-dynamic model.
The integration of active device and housing in a single technology process is desirable to eliminate manual adjustments in the µm range that are currently involved in the manufacturing process of conventional IMPATT diodes. Three thermo-compression bonding steps are necessary to fabricate a beamlead diode with a surrounding quartz ring on a heat sink. This leads to problems in reproducible manufacturing which is mandatory for power combining applications.

II. DIODE DESIGN

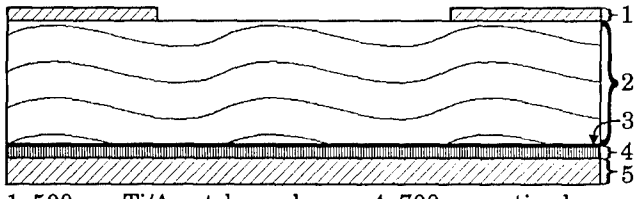
Optimization of RF-output power around the desired frequency of 150 GHz is the main goal. Hence, the design requires a low breakdown voltage in order to drive the diode with a high DC-current. This results in a high negative resistance. The limiting factor is the dissipated DC-power, which depends mostly on the quality of the bonding contact of the diode on the diamond heat sink. This leads to a DLHL diode design.
The doping levels and dimensions of the high field and drift regions are computer optimized with respect to their feasibility by the MBE. The minimum resolution of the growth rate and doping gradient of the MBE is close to the spike dimensions in the avalanche region of a DLHL profile for 150 GHz.
For simulation purposes, an in-house simulation tool [1] which is based on a hydro-dynamic carrier transport model is used. Simulations are carried out with a DC-current of 250 mA and a RF-voltage amplitude of 6 V at a 500K operating temperature. Results show that a diode diameter of 23 µm is a good compromise between high RF-output power and high impedance levels. The breakdown voltage gets as low as 8.5 V for the doping profile given in Tab. 1 with a maximum RF-output power of 220 mW at 150 GHz. The theoretical figures of RF-output power with and without considering series resistances of the diode are shown with measured RF-output power values in Fig. 5.

Tab. 1: Doping profile of integrated IMPATT diodes

150 GHz DLHL doping profile	doping concentration [cm^{-3}]	length [nm]
p - drift region	$2.2 * 10^{17}$	140
p^+ - spike	$1.4 * 10^{18}$	25
intrinsic		60
n^+ - spike	$1.5 * 10^{18}$	25
n - drift region	$1.2* 10^{17}$	150

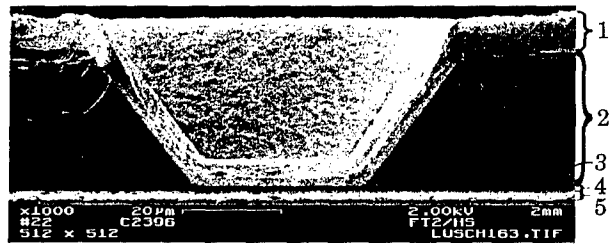
III. TECHNOLOGY PROCESS

The outstanding results obtained in [2,3] suggest a modification of the introduced beamlead diode process to fabricate housing and active device in a single technology process.
In [4], a successful realization of integrated IMPATT devices has been introduced for GaAs.
Instead of a low resistivity n^+-Si substrate, a high resistivity p^--SIMOX (*S*eparation by *Im*planted *Ox*ygen) substrate is used. This Si-substrate has a buried oxide layer, which acts primarily as an etch stop layer. It also improves isolation between the upper and the lower diode contact.
The active layer is grown by MBE on a 4" SIMOX wafer. The top is protected by an evaporated and electroplated 2 µm Ti/Au layer. This wafer is mechanically thinned and polished to a thickness of 100 µm. It is separated in 18x18 mm² pieces for better handling. The pieces are subsequently thinned by wet chemical etching in hot, aqueous KOH to a thickness of 30 µm.
The active layer then has to be contacted from the substrate side (n^+-contact). The following is a closer look at this critical process step.
A 370 nm thick, buried Si-oxide layer between the IMPATT diode layer and the Si-substrate is used as an etch stop layer. High etching selectivity for Si and SiO_2 in hot, aqueous KOH is reported in [5].
A Ti/Au etch mask with a thickness of 500 nm is structured lithographically, as shown in Fig. 1.
The via holes with a (111) crystal plane slope of 54.7 deg. are etched in the 29 µm thick Si-substrate in approximately 30 min. The etching process is basically stalled once the Si-oxide layer is reached.
For the buried oxide, an etch rate of about 5 nm/min is measured. This corresponds to the Si/SiO_2 etch selectivity given in [5] of about 250.
To make sure that the etch stop layer has been reached over the whole wafer, it is etched for another 10 min.
The etch-stop can be verified very easily with the microscope. The bottoms of the via-holes become green to blue once the oxide layer is reached. The Si-oxide is etched in buffered hydrofluoric acid. Only the Si-buffer layer and the active layer beneath it remain.



1: 500 nm Ti/Au etch mask
2: 29 µm p^--Si substrate
3: 370 nm SiO_2 etch stop layer
4: 700 nm active layer
5: 2 µm Ti/Au protection layer

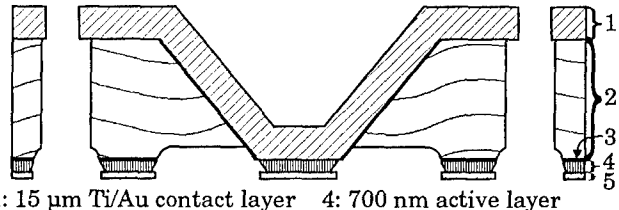
Fig. 1: Schematic of a wafer before via hole etching



1: 15 µm Ti/Au contact layer
2: 29 µm p^--Si substrate
3: 370 nm SiO_2 etch stop layer
4: 700 nm active layer
5: 2 µm Ti/Au protection layer

Fig. 2: SEM-picture of an etched and electroplated via hole

The Si-Buffer layer and parts of the oversized n^+-contact are removed by plasma etching to get deep into the n^+-contact region of the IMPATT diode.
Next, the top contact of the diode at the bottom of the via hole is defined.
This is achieved by evaporating a 300 nm thick Ti/Au-contact layer on the substrate side of the wafer. The devices are lithographically structured on the substrate side. The metal contact is then electroplated to a thickness of at least 15 µm to add stability to the thin wafer. This makes handling easier during the remaining process.
The thick metal layer is also needed to guarantee a good bond contact. The mesa diode is attached only to the upper gold contact. Thus, the bonding pressure that the diode experiences is determined by the thickness of the gold contact layer and the maximum pressure that the substrate is able to withstand.
The processed substrate side of the wafer is shown in a cross-section SEM picture in Fig. 2.
On the epitaxial side of the wafer mesas are defined by plasma etching using the lithographically structured contact metallization of the diode as an etch mask. As shown in Fig. 3, the active layer is utilized for two different purposes.
It is structured as a mesa diode and as a stand-off along the edges of the device. The stand-off is responsible for overall device stabilization on the heat sink and for diode protection. It seals the diode hermetically from the environment and prevents any exposure to mechanical stress.
In a last step, the wafer is plasma etched to separate the devices. The upper gold metallization is used as an etch mask.



1: 15 µm Ti/Au contact layer
2: 29 µm p^--Si substrate
3: 370 nm SiO_2 etch stop layer
4: 700 nm active layer
5: 300 nm Ti/Au etch mask and contact metallization

Fig. 3: Schematic of a cross-section view of the processed IMPATT device

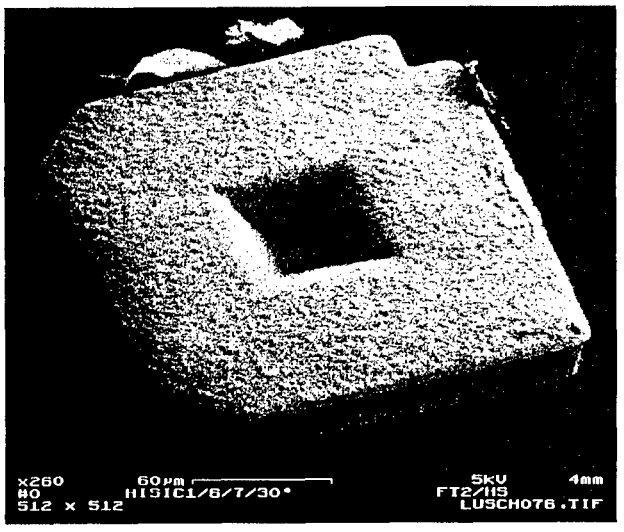


Fig. 4: SEM-picture of a top view of an integrated Si-IMPATT device for operation at 150 GHz

A SEM-picture of the final device is shown in Fig. 4. It is designed for operation at 150 GHz. It includes a diode with a diameter of 23 µm on the back side of the via-hole. The dimensions of the device are 200x200 µm^2 with a height of 45 µm.

IV. BONDING OF INTEGRATED DEVICES

The integrated diode is thermocompression bonded with a flat bondhead onto a diamond heat sink in a single step. The bond pressure has to be chosen carefully. On the one hand, it has to be high enough to assure a good bond contact and, thus, a good thermal connection between the IMPATT diode and the diamond. On the other hand, it must not exceed the maximum pressure that the Si-substrate is able to withstand. Tests show that bond pressures up to 2 bar can be applied without destroying the device. However, no major difference in the thermal resistance of devices that are bonded with 1.4 bar, 1.6 bar and 2 bar can be measured. They all show a thermal resistance of about 50 K/W. Bond contacts made with a lower pressure show higher values. For example, for a contact bonded with 1.2 bar a thermal resistance of 65 K/W is measured.
The following results are obtained with integrated diodes that are bonded with 1.4 bar for 15 sec. The typical thermal resistance measured with the method described in [6] is around 50 K/W.

V. MEASUREMENT RESULTS

RF characterization is carried out in a D-band waveguide resonator which is tuned at the reduced height end with a sliding short. The heat sink with diode is mounted in the waveguide resonator. Its position relative to the bottom of the waveguide can be varied with a micrometer screw. The diode is contacted by a choke from the top of the waveguide. Thin metal disks are put directly on top of the integrated device to match the impedance level of the diode to the resonator impedance. For tuning the frequency, disks with different diameters are used. Oscillations above 140 GHz require disks with diameters of 0.7 mm or smaller. Usually, for a fixed DC-current two diode positions with maximum RF-output power can be found. The diode is either elevated almost to the top of the waveguide or lowered about the height of the waveguide in its hole.
In Fig. 5, the measured results are shown. Additionally, the simulated theoretical RF-output power (—), which has a value of about 220 mW at 150 GHz, and the simulated RF-output power with series resistances of 1.0 (---) and 1.5 Ohms (-·-) is plotted. The RF-output power is reduced by more than 3 dB to 90 mW at 150 GHz when a series resistance of 1 Ohm is taken into account. A reduction of almost 10 dB to only 25 mW RF-output power at 150 GHz is the result of a series resistance of 1.5 Ohms. The latter corresponds to the measured series resistances of the characterized devices.
The series resistance needs to be improved during the next process runs to take full advantage of the potential of this doping profile. From experiences with the beamlead diode process a reduction to values between 1.0 and 0.5 Ohms is expected.
The actual measured values of several devices are marked with triangles. Test parameters are set to match the simulation results. The DC-current is 250 mA and only diodes with diameters of 23 µm are characterized.

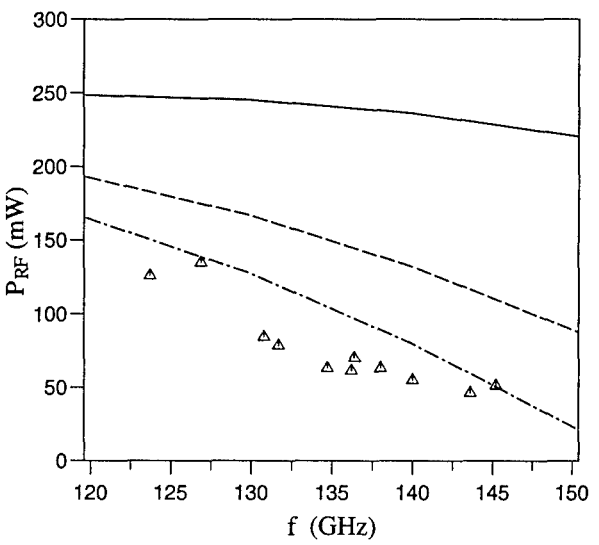


Fig. 5: Simulated and measured RF-output power of integrated IMPATT diodes; I_0=250 mA; U_1=6 V; T=500K; d=23 µm;
—: simulated diode RF-power without the inclusion of losses;
---: simulated diode RF-power with 1.0 Ohms series resistance;
-·-: simulated diode RF-power with 1.5 Ohms series resistance;
single triangles: measured oscillator RF-output power

In the region around 135 GHz the RF-output power is about 65 mW, above 140 GHz 50 mW can be achieved. This is in good agreement with the simulation values with a 1.5 Ohms series resistance. The minor differences between the measured power levels and the simulation results are due to surface resistance losses in the waveguide resonator setup.
The results show the desired progress in reproducibility. For unchanged current and tuning of the waveguide resonator, the operating points of the devices are close together.

VI. CONCLUSION

Integrated Si-IMPATT diodes for power combining applications at 150 GHz have been designed using computer optimization tools. The active layer is grown by MBE on a high resistivity SIMOX substrate. A new technology process for the fabrication of Si-IMPATT devices has been introduced in great detail. The process integrates the active element and its housing. The elimination of manual adjustments in the bonding of IMPATT diodes minimizes variations of device parameters caused during manufacturing. This makes the new integrated devices ideal candidates for power combining applications.
Simulation and measurement results of the integrated diodes have been presented. The measurement results show the desired match of the integrated devices. The low RF-output power of the devices from the first process run has to be blamed on series resistances introduced by the new process. A future challenge is the reduction of these series resistances.
Another topic is the design of a waveguide resonator that enables an exact and reproducible positioning of heat sinks for diode matching characterizations.

VII. ACKNOWLEDGEMENT

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